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A fully on-chip LDO voltage regulator with 37 dB PSRR at 1 MHz for remotely powered biomedical implants

Vahid Majidzadeh · Kanber Mithat Silay · Alexandre Schmid · Catherine Dehollain · Yusuf Leblebici

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Abstract This article presents a fully on-chip low-power LDO voltage regulator dedicated to remotely powered wireless cortical implants. This regulator is stable over the full range of alternating load current and provides fast load regulation achieved by applying a time-domain design methodology. Moreover, a new compensation technique is proposed and implemented to improve PSRR beyond the performance levels which can be obtained using the standard cascode compensation technique. Measurement results show that the regulator has a load regulation of 0.175 V/A, a line regulation of 0.024%, and a PSRR of 37 dB at 1 MHz power carrier frequency. The output of the regulator settles within 10-bit accuracy of the nominal voltage (1.8 V) within 1.6 μs, at full load transition. The total ground current including the bandgap reference circuit is 28 μA and the active chip area measures 290 μm × 360 μm in a 0.18 μm CMOS technology.

Keywords LDO voltage regulator · PSRR · inductive link · Cortical implants

1 Introduction

Minimally invasive monitoring of the electrical activity of specific cortical areas using implantable microsystems offers the promise of diagnosing neurological diseases, as well as detecting and identifying neural activity patterns which are specific to a behavioral phenomenon. Neural pattern classification and recognition require simultaneous recording from a large number of neurons [1–3]. However, extensive recording in-vivo requires full compliance with strict safety requirements. For example, the maximum temperature increase in brain tissue due to the operation of the implant should be kept at less than 1°C [4]. This requirement constrains the maximum allowable power dissipation in the implant, which reaches at most 4 to 5 mA drawn from a 1.8 V supply [5]. Moreover, electromagnetic absorption in the brain tissue also causes further temperature increase, which puts a constraint on the carrier frequency of the power link. Generally, this frequency is chosen in the range of 1 to 10 MHz in order to keep the absorption at minimum [6]. For this application, a 1 MHz power carrier frequency is chosen, which also decreases the interference between the power link and the data link (tuned at 40 MHz), as a benefit of the wider frequency separation [7]. Furthermore, biocompatibility of the package and the size of the implant should also be taken into account in order to avoid any adverse health effects. Specifically, the size constraint limits the number of discrete components and the chip area.

Figure 1 shows the block diagram of the wireless brain data acquisition system, which is composed of two main parts, the external reader and the implanted system. The external reader sends wireless power and control information to the implant, whereas the implanted device records the neural activity of a specific area of the brain and sends recorded data to the external system, again via inductive coupling. The far-field controller located in the external module communicates with a host computer or health center for chronical monitoring. The implantable IC includes a power conversion chain (PCC), a data

V. Majidzadeh (✉) · A. Schmid · Y. Leblebici
Microelectronic Systems Laboratory, Swiss Federal Institute of Technology EPFL, CH-1015 Lausanne, Switzerland
e-mail: vahid.majidzadeh@epfl.ch

K. M. Silay · C. Dehollain
RF-IC Group, Swiss Federal Institute of Technology EPFL, CH-1015 Lausanne, Switzerland

acquisition block, and a transmitter. The issues related to wireless power transmission and inductive link design have been tackled in other publications by the authors, and will not be discussed here [7–9]. The PCC, which is enclosed in the shaded box of Fig. 1, is composed of a resonance tank, a rectifier and a voltage regulator. The resonance tank is tuned to 1 MHz, which is the carrier frequency of the inductive link. Further in the PCC chain, the voltage rectifier performs the AC/DC conversion and finally, the voltage regulator filters out residual ripples.

The voltage regulator is a key element of the PCC, which should exhibit high PSRR at carrier frequency, low standby current, low drop-out voltage, monolithic integration, and stable operation at low load current [10, 11]. Moreover, the output of the voltage regulator is directly used as a reference voltage for analog blocks, including a 10-bit SAR ADC where high accuracy as well as fast line and load transient responses are also extremely important. In absence of this condition, dedicated voltage buffers are required to provide accurate reference voltages which may increase the system total power consumption.

Conventional voltage regulators typically use a large off-chip capacitor, of up to 10 μF, as a critical element for regulation and stability [12, 13]. Thus, they are not suitable for implantable applications considering the area/volume constraints. Recently, several techniques have explored the effectiveness of fully on-chip solutions. Nonetheless, existing solutions only partially address the aforementioned issues. The damping frequency compensation technique provides high PSRR (−30 dB at 1 MHz) in [14], but the regulator is unstable at low load current. In [15], a derivative feedback path guarantees the stability at the expense of additional active circuitry and a ground current of 65 μA. Cascode compensation with dynamic bandwidth boosting is proposed in [16], which guarantees stability over the full range of alternating load current, at the cost of increased power consumption.

In this paper, we demonstrate that a symmetric single-ended cascode compensation technique can be used to stabilize the regulator over the full range of alternating load current, thereby eliminating the need of any additional active circuitry [15] or a dynamic bandwidth boosting technique [16]. In order to minimize the ground current, optimum pole-zero allocation of the loop gain transfer function has been investigated in time domain rather than in the frequency domain. Moreover, a novel technique is introduced to enhance the PSRR beyond the performance which can be achieved using classical cascode compensation technique.

This paper is organized as follows. Section 2 describes the proposed voltage regulator. In Sect. 3, the bandgap reference circuit including the power-on-reset and start-up circuitry is presented. Section 4 presents measurement results of the standalone voltage regulator and characterization results with the inductive power link, and Sect. 5 concludes the paper.

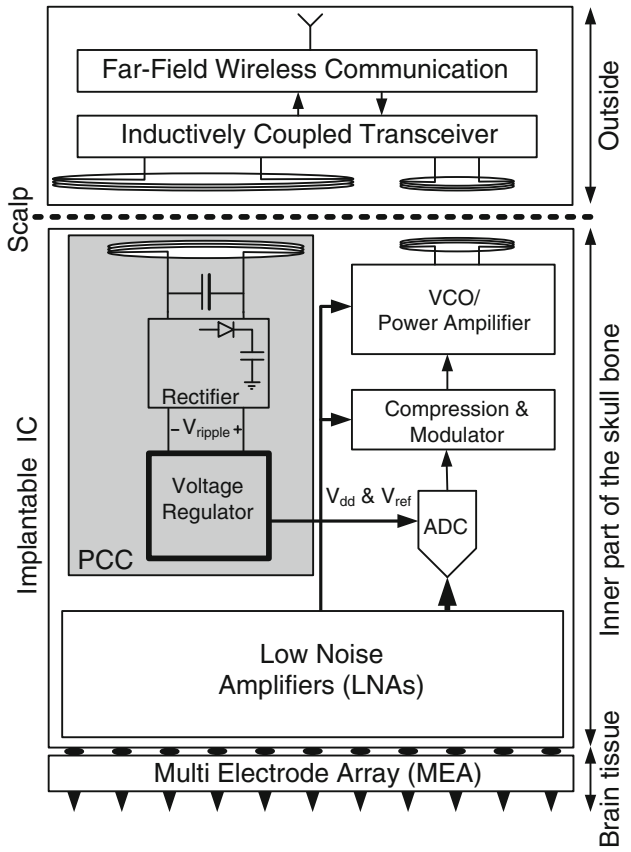

Fig. 1 Block diagram of the wireless brain data acquisition system

2 Proposed voltage regulator

Figure 2a shows the overall architecture of the on-chip voltage regulator. No external component is required in this architecture, which reduces the total cost and facilitates the system installation in-vivo. In order to keep voltage overshoots and undershoots reasonably bounded in conditions of fast load transients, a 100 pF MOS capacitor is integrated on-chip at the output of each regulator stage to act as an instantaneous charge source. Larger values of the on-chip load capacitances reduce the voltage overshoots and undershoots in large load transitions at the cost of reduced phase margin and stability. The supply voltage denoted as V_{ripple} is provided by the rectifier output, and can be as low as 2.1 V in order to provide an output voltage, $V_{out} = 1.8$ V, while maintaining the PSRR performance. A closed-loop power control circuitry is indispensable to control the power delivered by the external class-E power amplifier driving

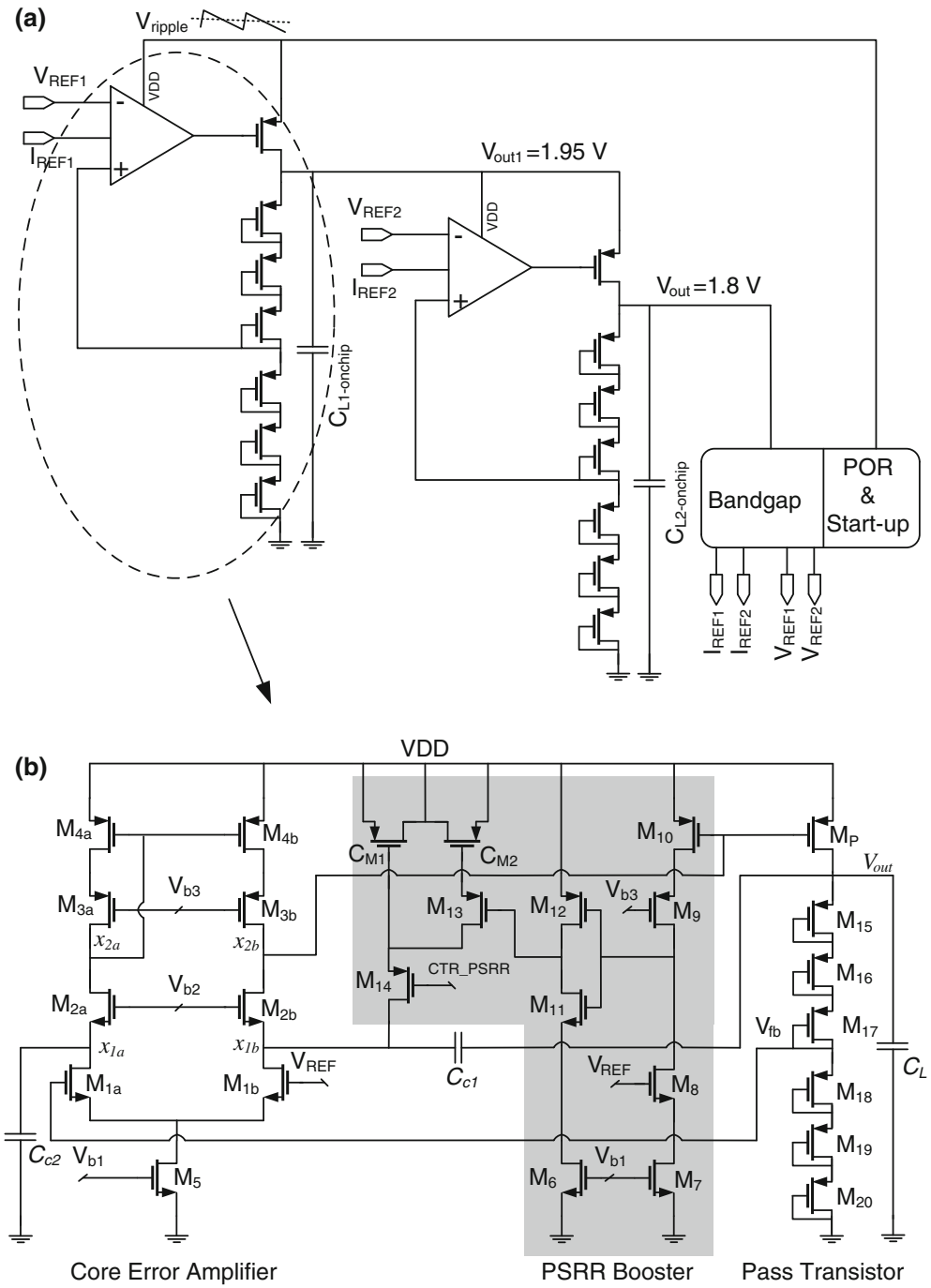

Fig. 2 **a** Architecture of the fully on-chip voltage regulator, **b** circuit schematic of the first stage

the primary power coil, in order to guarantee a minimum value of 2.1 V at the output of the rectifier [9].

Two-stage cascaded regulation is used and both stages are identical, only differing in their reference voltages V_{REF1} and V_{REF2}. The cascaded regulator architecture benefits from enhanced PSRR at the cost of an increased voltage drop and a degraded power efficiency of the voltage regulator. Sub-threshold MOS transistors are utilized as a feedback network instead of conventional polysilicon or N-well resistors in order to save standby current and silicon area. The number and size of the devices control the standby current passing through the MOS transistors ladder. The worst-case design scenario in terms of stability (slow process corner) is used to guarantee enough phase margin of the loop. A larger standby current value (several hundreds of nano-amperes) in fast process corners enhances the stability, and is negligible in comparison with the bandgap current flowing through the pass transistor M_P.

Indeed, the bandgap current drained through the pass transistors provides enough phase margin to guarantee stability, even at no load condition.

A bandgap reference circuit with dynamic power-on reset circuitry is used to generate the required reference voltages and currents. The bandgap is supplied from the regulator output, which mitigates the need for high PSRR reference voltage generation.

Figure 2b shows the circuit schematic of the first stage, including the improved frequency compensation and PSRR enhancement circuitry, which is shown in the shaded box. The reference current I_{REF1} provided by the bandgap reference is fed to the bias circuitry, which in turn generates the bias voltages V_{b1-3}. The bias circuit is not shown, for the sake of simplicity. The core of the error amplifier consists of a single-ended telescopic cascode amplifier using C_{c1} and M_{2b} as compensation network. Since the source terminal of M_{2b} is a low-impedance node, C_{c1} operates as a derivative element and provides fast feedback in current mode ($i \approx C_{c1} \cdot dV_{out}/dt$) [16]. However, this compensation technique creates asymmetric left-half plane (LHP) and right-half-plane (RHP) zeros with varying load, which degrades the transient response. Dynamic bandwidth boosting proposed in [16] pushes these asymmetric LHP/RHP zeros to higher frequencies when the load current increases, at the cost of increasing ground current. Another solution suitable for avoiding these asymmetric zeros consists of canceling the feed-forward path created by the compensation capacitor C_{c1}, using a dedicated active pseudo-differentiator feedback at the cost of increased power consumption [15]. In this work, we propose a simple passive solution making use of C_{c2} as an auxiliary compensation capacitor, which does not cause any power penalty.

2.1 Frequency response

As schematically depicted in Fig. 3, two issues emerge in the frequency and time-domain analysis of on-chip regulators when the off-chip capacitor is eliminated or replaced with a small on-chip integrated capacitor. In frequency domain, the dominant pole cannot be placed at the output of the regulator. Thus, an effective compensation technique is required to place the dominant pole inside the loop, and move the parasitic pole located at the output to high frequencies. In time domain, large overshoots and undershoots appear in the load transient response due to the lack of instantaneous charge source [15]. Therefore, a fast feedback network is necessary to adapt the gate voltage of the pass transistor.

Considering the pass transistor in Fig. 2b as a single-stage common-source amplifier, the complete circuit acts as a two-stage amplifier with very large variation of the DC operating point of the second stage. Cascode compensation, which is more effective than Miller compensation [17], stabilizes the loop in spite of this large variation of the DC operating point. Figure 4 shows the equivalent small-signal model of the voltage regulator excluding the PSRR booster. The resistor r_1 corresponds to the equivalent lumped output resistance at node x_{2b} of Fig. 2b, R_L and C_L are the equivalent output resistance and capacitance, g_{m1}, g_{m2}, g_{m4}, and g_{mp} represent the transconductance of $M_{1a,b}$, $M_{2a,b}$, $M_{4a,b}$ and M_p respectively. The parasitic capacitances c_{gs} and c_{gd}, refer to the parasitic gate capacitances of the pass transistor M_p. It can be easily shown that without the auxiliary compensation capacitor C_{c2} and considering that $C_L > C_{c1} + c_{gd}$, the open-loop transfer function is expressed as follows:

$$H(S) = g_{m1} r_1 \cdot g_{mp} R_L \frac{1 + b_1 S + b_2 S}{1 + a_1 S + a_2 S^2 + a_3 S^3} \tag{1}$$

where

$$b_1 \approx \frac{C_{c1}}{2 g_{m2}}, \; b_2 = -\frac{C_{c1} c_1}{2 g_{m2} g_{mp}},$$

$$a_1 = r_1 \left(C_{c1} + c_{gd}\right) g_{mp} r_p + \frac{C_{c1}}{g_{m2}} + r_1 c_1 + R_L C_L$$

$$a_2 = r_1 c_1 R_L C_L + R_L C_L \frac{C_{c1}}{g_{m2}} + r_1 \left(c_1 + g_{mp} r_p c_{gd}\right) \frac{C_{c1}}{g_{m2}},$$

$$a_3 = c_1 r_1 C_L R_L \frac{C_{c1}}{g_{m2}} \tag{2}$$

and $c_1 = c_{gs} + c_{gd}$. Since $g_{mp} > g_{m2}$ and $C_{c1} > c_1$, two asymmetric zeros are created in the open-loop transfer function:

$$\omega_{z1} \approx -\frac{1}{\tau_{z1}} = -\frac{2 g_{m2}}{C_{c1}}, \quad \omega_{z2} \approx -\frac{1}{\tau_{z2}} = \frac{g_{mp}}{c_1} \tag{3}$$

Increasing the load current, and consequently g_{mp}, the RHP zero and the non-dominant pole formed at the circuit output move to higher frequencies, while the unity-gain frequency and the LHP zero almost remain unchanged. This results in an excess phase injected into the loop at large load currents, which dramatically slows down the transient response. Figure 5a illustrates the frequency response of the loop at no-load and full-load (4 mA) conditions. The observed large peaking of the phase response at full-load state seen in this figure confirms the aforementioned statements. This issue could be mitigated by pushing the LHP zero to high frequencies when load current increases, at the cost of increased power dissipation [16]. The proposed solution in this study consists of using an auxiliary capacitor C_{c2}. Using $C_{c2} = C_{c1} = C_c$, the resultant transfer function sees its poles remaining unchanged, while zeros relocate to the following symmetrical locations:

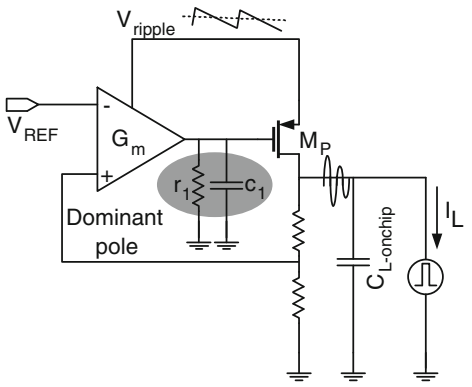

Fig. 3 Description of the dominant pole and large transient overshoots in the on-chip LDO voltage regulator

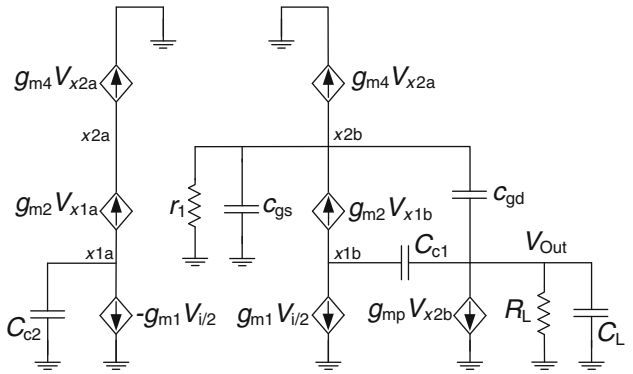

Fig. 4 Equivalent small-signal model of the voltage regulator, excluding the PSRR booster

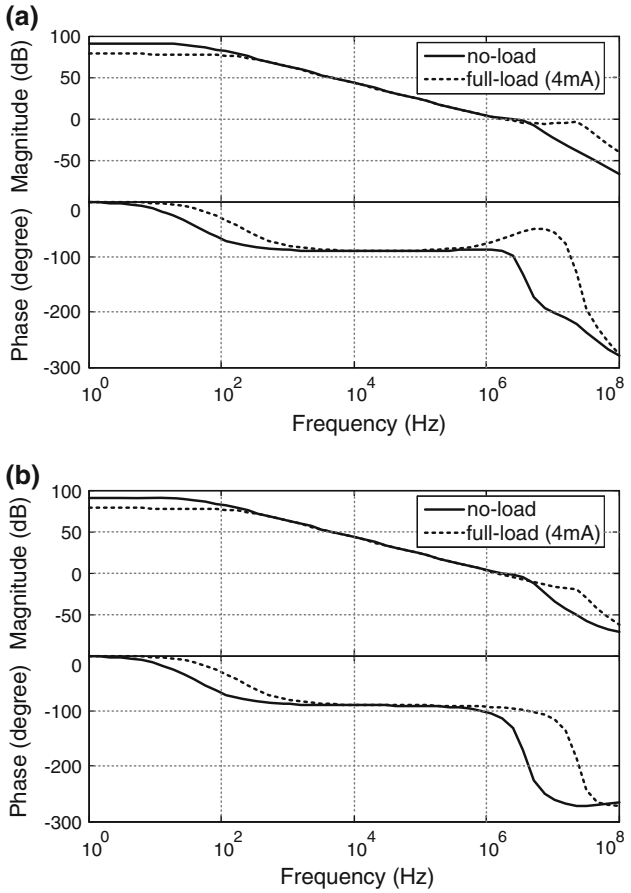

Fig. 5 Frequency response of the regulator, **a** without auxiliary capacitor C_{c2}, **b** with auxiliary capacitor C_{c2}

$$\omega'_{z1,z2} = \mp\frac{1}{\tau'_{z1,z2}} = \pm\sqrt{\frac{2g_{m2}g_{mp}}{c_1 C_{c1}}} \tag{4}$$

It is quite obvious that by increasing the load current, and consequently g_{mp}, the zeros are moved to higher frequencies at identical rate. This improvement is illustrated in Fig. 5b, where increasing the load current is observed to have a negligible effect on the phase margin and the related transient response.

2.2 Design methodology

Since the output of the voltage regulator is used as a reference voltage for analog blocks, the transient response and settling behavior are very critical. Special considerations are necessary to find an optimum solution in terms of power and speed. In this study, a time-domain design methodology is developed, which results in minimum power consumption for a desired settling behavior. Figure 6 shows the open-loop pole-zero location of the system transfer function derived in (1) and the corresponding closed-loop pole-zero location. The closed-loop transfer function is analyzed in order to characterize the transient response of the regulator.

$$H_{cl}(S) = \frac{1}{\beta_0}\frac{\left(1+\tau'_{z1}S\right)\left(1+\tau'_{z2}S\right)}{\left(1+\frac{1}{\omega_{cl}}S\right)\left(1+\frac{2\xi}{\omega_n}S+\frac{1}{\omega_n^2}S^2\right)} \tag{5}$$

where β_0 is the feedback factor (here $\beta_0 = 0.5$), τ'_{z1} and τ'_{z2} are time constants related to the symmetric zeros in (4). The real pole, ω_{cl}, natural frequency, ω_n, and damping factor, ξ, are related to circuit parameters as follows:

$$\omega_{cl} \approx \beta_0\frac{g_{m1}}{C_{c1}},\ \omega_n \approx \sqrt{\frac{g_{m2}g_{mp}}{c_1 C_L}},\ \xi \approx \frac{1}{2}\left(A\sqrt{\frac{\tau_2}{\tau_3}}+B\sqrt{\frac{\tau_3}{\tau_2}}\right) \tag{6}$$

where

$$\tau_2 = \frac{c_1}{g_{m2}},\ \tau_3 = \frac{C_L}{g_{mp}},\ A = \frac{1}{g_{mp}R_L},\ B = \frac{1}{g_{m2}r_1}+\frac{c_1}{C_{c1}} \tag{7}$$

The transient behavior of the regulator is characterized by its step response and its associated settling error. The percentage settling error at the regulator output at a specific time t_s is expressed in (8). For simplicity, the effect of the

zeros in (5) is ignored; still, a closed-form mathematical expression of the settling error in presence of the zeros can be expressed, at the cost of increased mathematical complexity.

$$e_{ss} = \frac{I_{\text{full}}\Delta t}{C_L V_{\text{out}}}\left\{\frac{e^{-\alpha\xi\omega_n t_s}}{1-2\alpha\xi^2+\alpha^2\xi^2}+\frac{\alpha\xi e^{-\xi\omega_n t_s}}{1-2\alpha\xi^2+\alpha^2\xi^2}\right. \times\left[(-2\xi+\alpha\xi)\text{Cos}\left(\omega_n t_s\sqrt{1-\xi^2}\right).\right. +\left.\left.\left(\frac{1-2\xi^2+\alpha\xi^2}{\sqrt{1-\xi^2}}\right)\text{Sin}\left(\omega_n t_s\sqrt{1-\xi^2}\right)\right]\right\} \tag{8}$$

where $\alpha = \omega_{cl}/\xi\omega_n$ is the ratio of the real pole to the real part of the complex pole as shown in Fig. 6b, $V_{\text{out}} = 1.8$ V is the nominal output voltage, $I_{\text{Full}} = 4$ mA refers to the instantaneous full-load current drained from the output, and Δt is the rising time of the transient load current. A two-step optimization process adapted from [18] is used to derive the optimum parameters α and ξ. Figure 7 shows the percentage of the settling error versus the normalized parameter $\omega_n t_s$. The optimization is performed in the following two steps. In the first step, the optimum damping factor ξ is obtained for a fixed value of α. The optimum value is the one which minimizes the power consumption ($\omega_n t_s$) for a given settling accuracy. In the second step, the damping factor ξ is fixed to the optimum value obtained in the first step, and parameter α is optimized. The optimization process results in $\xi = 0.55$ and $\alpha = 1.1$ for 10-bit accuracy (0.1% settling error) and minimum power consumption. The sensitivity of the settling accuracy to pole-zero locations, ξ and α, should also be taken into account during the optimization process. Increasing the damping factor of complex poles ξ, the less sensitive settling behavior is achieved at the cost of increased power consumption for a given speed requirement, t_s. Given the optimum pole-zero location parameters $\omega_n t_s$, α, and ξ, the values of circuit parameters in (6) and (7) are derived.

2.3 Power supply rejection ratio

PSRR is one of the most important specifications for remotely powered implantable devices, especially at the frequency of the power carrier. Special considerations have to be taken into account both at the circuit and system levels. Multistage voltage regulation and supplying the bandgap reference from the regulated voltage are implemented as system-level solutions.

At circuit level, the architecture of the error amplifier and the compensation scheme affect PSRR. Cascode compensation is not only effective in terms of pole splitting in comparison to Miller compensation, but also is beneficial in terms of PSRR [17]. In this work, a new technique is proposed which improves PSRR beyond the performance which can be achieved by cascode compensation. The circuit is shown in the shaded box of Fig. 2b, which is referred to as PSRR booster. The simplified circuit schematic of the regulator and small-signal model of the PSRR booster are shown in Fig. 8. In this model, C_{ps} is the equivalent compensation capacitor formed by C_{M1} and C_{M2}, r_p indicates the output resistance of the pass transistor M_p, and R_L stands for the equivalent load resistance. Intuitively, a gate-source voltage fluctuation of M_p due to supply noise is reduced by reproducing the supply noise at the gate terminal of M_p. Since $C_{ps} \ll C_{c1}$, the main frequency response of the error amplifier is not affected.

$$H_{ps}(S) = \frac{V_{\text{out}}(S)}{V_{dd}(S)} \approx g_{mp}R_L \cdot \frac{\left(1+\frac{C_c}{g_{m2}}S\right)(1+\gamma' S)}{1+a_1 S+a_2 S^2+a_3 S^3} \tag{9}$$

where

$$\gamma' = \gamma - \left(\frac{C_{ps}\cdot g_{mp}r_p}{1+g_{mp}r_p}\right)r_1 + \frac{C_{ps}}{g_{m2}}, \quad \gamma = \left(c_{gdp}+\frac{c_{gsp}}{1+g_{mp}r_p}\right)r_1 \tag{10}$$

Without compensation ($C_{ps} = 0$ and $\gamma = \gamma'$), the dominant zero is determined by the time constant γ. When the

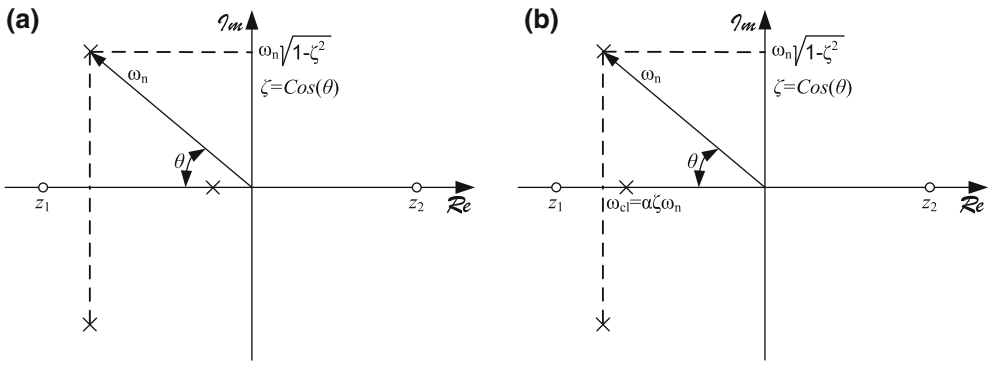

Fig. 6 Pole-zero location of the voltage regulator, **a** open-loop, **b** closed-loop

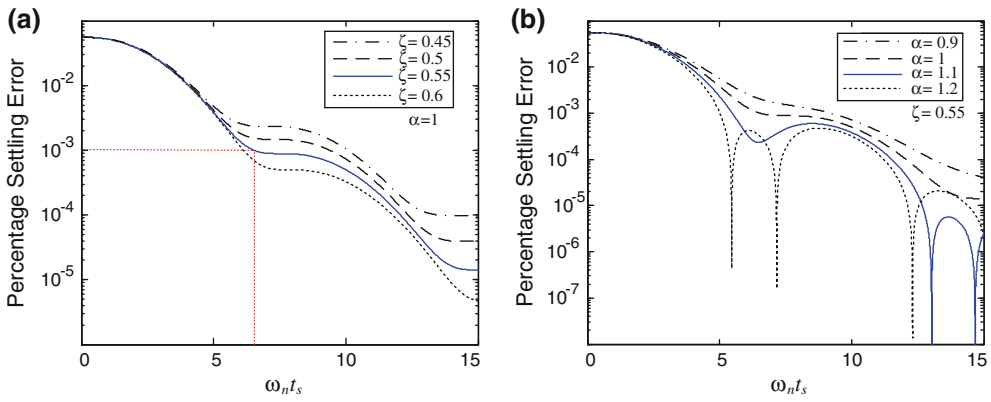

Fig. 7 Percentage of the settling error versus the normalized parameter $\omega_n t_s$, **a** $\alpha = 1$ and ξ is swept, **b** $\xi = 0.55$ and α is swept

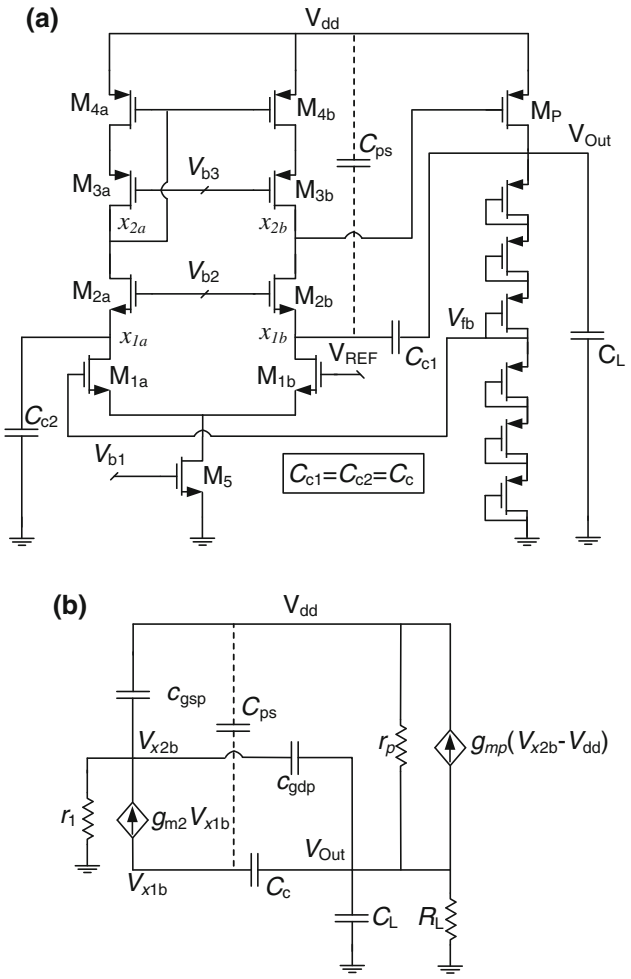

Fig. 8 **a** Simplified circuit schematic of the regulator, **b** small-signal model of the PSRR booster

compensation technique is applied, the negative time constant formed by C_{ps} is subtracted from the time constant of the dominant zero. Consequently, the dominant zero moves to higher frequencies resulting in higher roll-up frequency. The optimum value of C_{ps} tracks the time constant represented by γ under process and load variations.

$$C_{ps} = \frac{c_{gdp}\left(1 + g_{mp}r_p\right)}{g_{mp}r_p} + \frac{c_{gsp}}{g_{mp}r_p} \approx \begin{cases} c_{gdp} & \text{no} - \text{load}, g_{mp}r_p \gg 1 \\ 2c_{gdp} + c_{gsp} & \text{full} - \text{load}, g_{mp}r_p \approx 1 \end{cases} \quad (11)$$

Obviously, the optimum value of C_{ps} depends on the load current. Thus, an adaptive compensation network is required. Fig 2b shows the adaptive compensation technique realized by a two-level adaptation circuit M_{6-13}, with a level-switching threshold load current at 1.6 mA. Transistor M_{14} acts as a control switch: when the control signal CTR_PSRR is low, the proposed technique is applied; otherwise it is disabled. A very small fraction of the pass current (0.1%) is copied by M_{10} and is compared with the reference current of M_7. If it exceeds 1.6 mA, C_{M2} is activated; otherwise only C_{M1} is operational. M_6 limits the maximum short-circuit current of M_{11-12} to a reasonable value of 1.6 μA at the switching point.

3 Bandgap reference

The reference voltages and currents required for error amplifiers are provided by a bandgap reference shown in Fig. 9 with start-up and power-on-reset circuitry. The reference voltages are achieved by summation of two PTAT and CTAT currents I_1 and I_2 [19]. Resistor R_6 is used to alleviate the need for a dedicated bias circuit to generate V_{p2}, and resistor R_7 is used to improve the matching in the current mirrors and enhance the PSRR of the bandgap reference; $M_{6a,b}$ provide the reference bias current needed in the bias circuit of the error amplifiers; and finally, the current copied through M_4 generates reference voltages of 0.9 V and 0.975 V. The ratio of the R_1 and R_3 and aspect ratios of m and n are chosen such that first order thermal compensation is achieved.

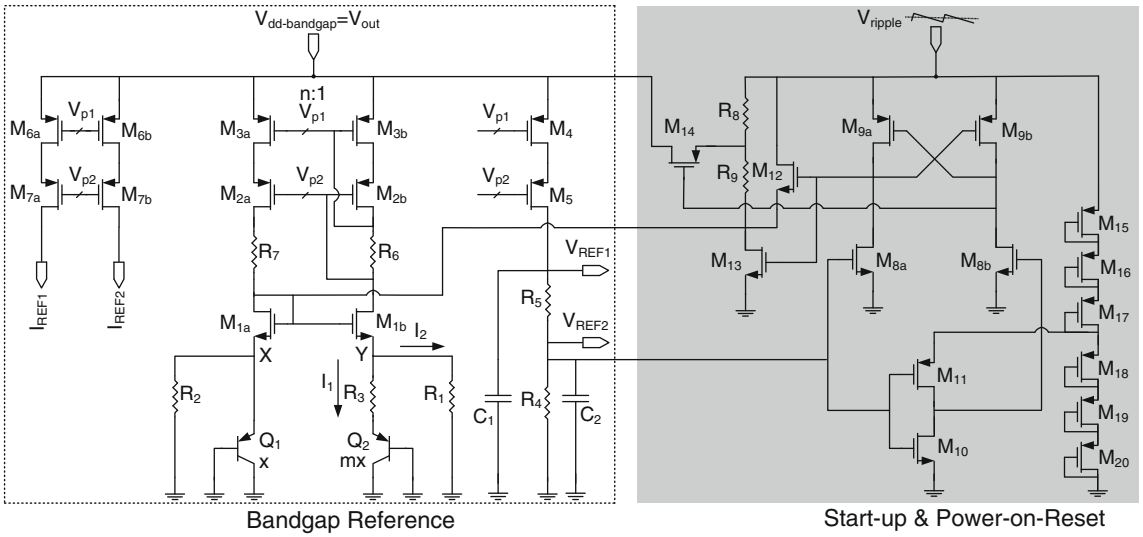

Fig. 9 Bandgap voltage reference with start-up and power-on-reset circuitry

A start-up and power-on-reset circuit is essential in order to avoid the second stable operating point of the bandgap ($I_1 = I_2 = 0$), and provide the initial power supply for the bandgap. M_{8-11} generates the differential control signals for the start-up and power-on-reset circuit. Concurrently, it also acts as a low-to-high voltage converter to cancel the static current in normal operation. The low-level supply required by M_{11} is provided by the subthreshold MOS ladder M_{15-20}. A careful sizing of the devices is required to prevent a large current increment through the MOS ladder in fast corners of the process. M_{12} acts as start-up device and M_{13-14} along with R_{8-9} constitute the power-on-reset circuit. When the power supply is rising, V_{REF2} is low, and the gate voltage of M_{12-13} increases while the gate voltage of M_{14} remains low. Then, M_{12} pulls the gate voltage of M_1 up. In the meantime, the core of the bandgap circuit is supplied by the voltage provided by the resistor ladder R_{8-9}. When V_{REF2} reaches close to 0.9 V, the latched inverter M_{8-9} turns M_{12-14} off and M_{13} shuts down the static current flowing through R_{8-9}. The ratio of R_{8-9} is chosen such that zero voltage switching can take place for increased reliability.

4 Experimental results

4.1 Stand-alone voltage regulator characteristics

The regulator circuit has been realized in a 0.18μm CMOS technology, and experimentally characterized [20]. Figure 10 shows the microphotograph of the voltage regulator with an active chip area of 290 μm × 360 μm, which is dominated by on-chip MOS capacitors.

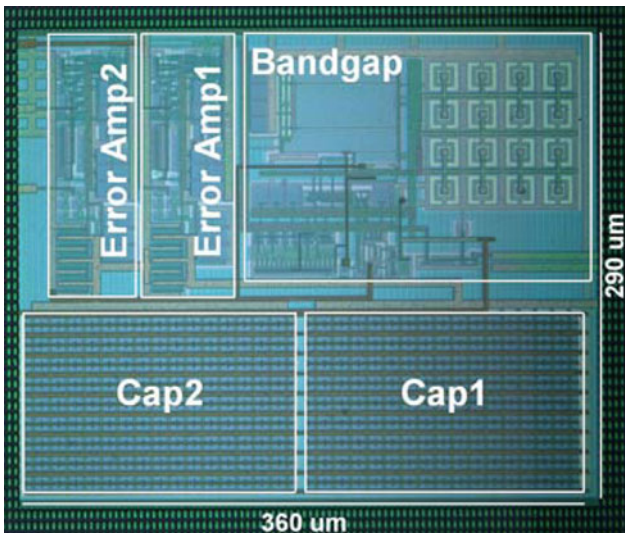

Fig. 10 Microphotograph of the active area of the voltage regulator chip

Figure 11 shows the measured supply voltage gain at 2 mA load current. Without boosting, PSRR is 33.7 dB at 1 MHz, while it reaches 37 dB when the boosting technique is applied which shows 3.3 dB improvement. The PSRR improvement obtained at 1 MHz in post-layout simulations is 8.3 dB. The measured improvement is 5 dB less than values predicted from simulations, due to extra parasitic capacitance on the gate node of pass transistor M_p. Figure 12 shows the measured supply voltage gain versus load current at 1 MHz. PSRR improvement is preserved through the entire dynamic range of the load current by using two-level adaptation, with a switching point centered at 1.6 mA.

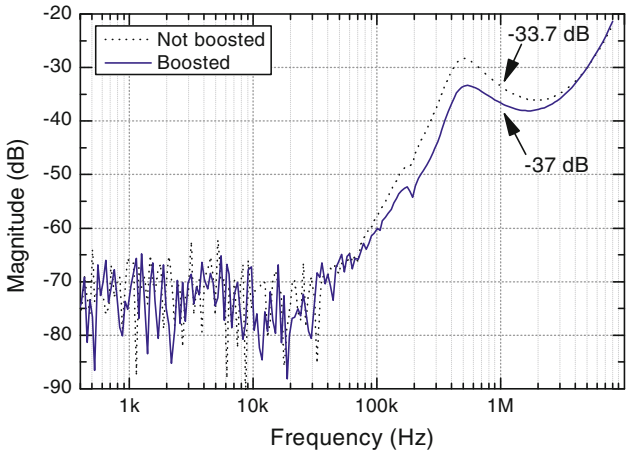

Fig. 11 Measured supply voltage gain with (*solid*) and without (*dotted*) PSRR boosting technique

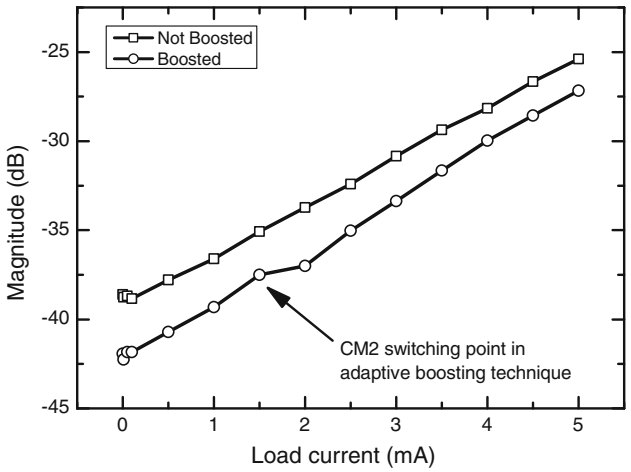

Fig. 12 Measured supply voltage gain versus load current at 1 MHz

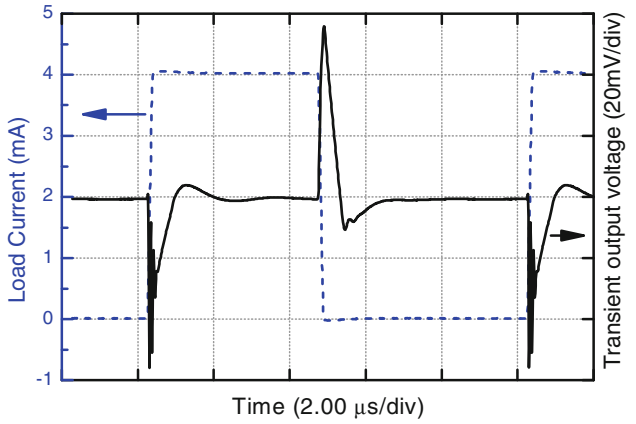

Fig. 13 Measured load transient response when load current rises from 0 to 4 mA within 200 ns

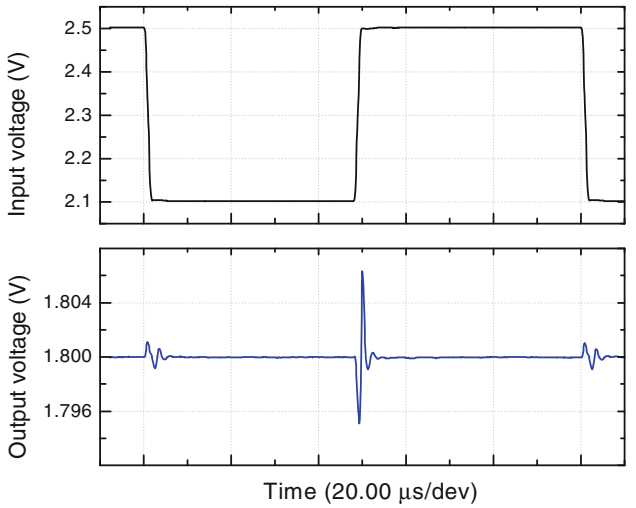

Fig. 14 Measured line transient response in full load condition

Figure 13 shows the measured load transient response when the load current increases from 0 to 4 mA within 200 ns. The settling time for 0.1% accuracy is 1.6 µs, which enables the use of this unit as a reference voltage for an embedded 10-bit ADC. The measured load regulation is 0.7 mV for a 4 mA load current. Figure 14 shows the line transient response measured for 400 mV_{p-p} steps with 2 µs rise and fall time in full-load condition. The worst-case line regulation measured in this experiment is 97 µV/400 mV, which is a promising result for burst-mode powering applications such as inductively powered circuits.

The measured output spot noise is 1.1 $\mu V/\sqrt{Hz}$ at 100 Hz and decays to 390 $nV/\sqrt{Hz}$ at 100 kHz. The total current sink from the 2.1 V rectifier output is 28 µA, where the major contributor is the bandgap reference circuit which consumes 16 µA. Table 1 shows the summary of the results and comparison with the state-of-the-art published on-chip voltage regulators, demonstrating the optimal applicability of the proposed regulator for implantable applications, where low-power consumption, small silicon area, high PSRR, and good line/load regulation are demanded.

4.2 Characteristics with the inductive link

The voltage regulator is also characterized with the inductive power link presented in [8]. Figure 15 shows the measurement setup for the inductive power link. It is composed of power coils, a matching network, a rectifier, and the on-chip voltage regulator. The matching network is used to enhance the overall power transfer efficiency and boost the voltage amplitude of the power carrier at the input of the voltage rectifier. The power carrier is applied to the input of the inductive link using an off-the-shelf unity-gain buffer, and the load of the regulator is adjusted with a variable resistor.

Table 1 Summary of performance and comparison with other works

Parameter	[2]	[3]	This work
Technology (CMOS)	0.6 μm	0.35 μm	0.18 μm
Drop voltage	200 mV	200 mV	300 mV
Ground current	38 μA	65 μA	28 μA
Bandgap included	yes	no	yes
Load regulation	–	40 mV/50 mA	0.7 mV/4 mA
Line regulation	0.15%	0.3%	0.024%
Stability range	$I_L > 10$ mA	Full load	Full load
Settling time	2 μs	15 μs	1.6 μs
Accuracy	Not mentioned	Non mentioned	10-bit
PSSR at			
1 kHz	60 dB	57 dB	70 dB
1 MHz	30 dB	–	37 dB
Spot Noise at			
100 Hz	$1.8\mu V/\sqrt{Hz}$	$4.6\mu V/\sqrt{Hz}$	$1.1\mu V/\sqrt{Hz}$
100 kHz	$380nV/\sqrt{Hz}$	$630nV/\sqrt{Hz}$	$390nV/\sqrt{Hz}$
Active chip area	568 μm × 541 μm	538 μm × 538 μm	290 μm × 360 μm

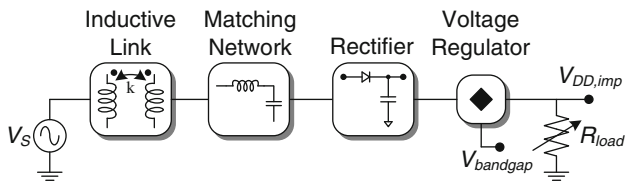

Fig. 15 Measurement setup for the inductive power link

The coils of the inductive link are fabricated on printed circuit boards. Figure 16 shows the photograph of the orthogonally arranged power and data coils [7]. The implanted power coil measures 10 mm × 10 mm and has an inductance of 673.2 nH, while, the external reader power coil occupies a 42 mm × 42 mm area and has inductance of 86.7 μH. The coils are placed at a distance equal to 5 mm with a measured coupling factor of approximately 0.12 for dry air interface. The rectifier and matching network are implemented on the backside of the implanted power coil using off-the-shelf components. The complete package for the cortical implant is presented in [9].

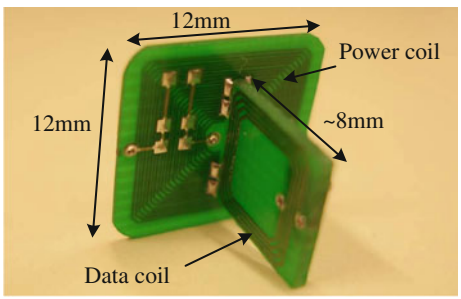

Fig. 16 Photograph of the orthogonally arranged power and data coils for the implantable side [7]

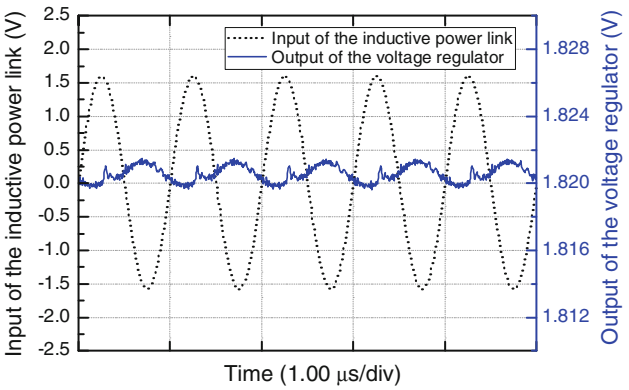

Fig. 17 Measured transient response of the voltage regulator powered with the inductive link

Figure 17 shows the transient response of the voltage regulator powered with the inductive link for a 1.83 mA load current. The input of the voltage regulator is kept at 2.2 V in this measurement. The maximum ripple voltage at the output is measured as 1.88 mV when the voltage regulator operates with the inductive power link. The voltage regulator efficiency is measured to be 80% on the overall range, and the maximum power transfer efficiency achieved from the complete inductive link is 17.4%, which is dominated by the resistive losses of the coils and the small coupling factor.

5 Conclusion

A fully on-chip LDO voltage regulator for remotely powered cortical implants is presented. The regulator circuit

design features an improved symmetric single-ended cascode compensation, which guarantees the stability through the full load current range. Moreover, a novel technique is introduced to boost the PSRR compared to conventional cascode compensation technique. A load regulation of 0.175 V/A and a line regulation of 0.024% have been measured. The regulator is stable through the full load range and settles within 10-bit accuracy of the nominal voltage within 1.6 μs under full load current transition. The PSRR at 1 MHz is measured at 37 dB using the proposed PSRR booster circuit. The regulator is fabricated in a 0.18 μm CMOS technology and drains 28 μA from the supply. The active chip area is 0.105 mm^2. The proposed voltage regulator is experimentally characterized with an inductive power link with small form factor developed for implantable applications. The measured power transfer efficiency is 17.4%, which is limited by the small coupling factor and resistive losses in primary and secondary coils. With these characteristics, the presented regulator is uniquely suitable for implanted applications where highly accurate and stable reference voltages are needed.

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Vahid Majidzadeh received the M.S. degree in Electrical Engineering from University of Tehran, Tehran, Iran, in 2006. From 2005 to 2006 he was with NikTek semiconductor as an analog design engineer, where he was involved in the design of high-resolution delta-sigma ADCs for precision audio systems. In 2007 he joined Microelectronic System Laboratory (LSM) in Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. Currently he is pursuing Ph.D degree working on low-power mixed-signal circuits and implantable transceivers for biomedical applications.

Kanber Mithat Silay was born in Konya, Turkey, in 1982. He received the B.S. and M.S. degrees in Electrical and Electronics Engineering from Middle East Technical University (METU), Ankara, Turkey, in 2004 and 2006, respectively. Currently, he is pursuing the Ph.D. degree in microsystems and microelectronics at Ecole Polytechnique Fédérale de Lausanne (EPFL). His research interests include wireless telemetry and remote powering for cortical implants, low-power analog integrated circuit design, and radio-frequency integrated circuits.

Alexandre Schmid received the M.S. degree in Microengineering and the Ph.D. degree in Electrical Engineering from the Swiss Federal Institute of Technology (EPFL) in 1994 and 2000, respectively. He has been with the EPFL since 1994, working at the Integrated Systems Laboratory as a research and teaching assistant, and at the Electronics Laboratories as a post-doctoral fellow. He joined the Microelectronic Systems Laboratory in 2002 as a Senior Research Associate, where he has been conducting research in the fields of non-conventional signal processing and neuromorphic hardware, reliability of nanoelectronic devices, and bioelectronic and brain-machine interfaces, and also teaches at the Microengineering and Electrical Engineering Departments of EPFL. Dr. Schmid has published over 70 refereed papers in journals and conferences. He has served as the General Chair of the Fourth International Conference on Nano-Networks in 2009, and serves as an Associate Editor of the IEICE Electronics Express since 2009.

Catherine Dehollain received the degree in Electrical Engineering in 1982 and the Ph.D. degree in 1995, both from the Swiss Federal Institute of Technology in Lausanne (EPFL), Lausanne, Switzerland. From 1982 to 1984, she was a Research Assistant at the Electronics Laboratories (LEG), EPFL, where she was engaged in designing switched capacitor filters and studying MOS transistor modeling. In 1984, she joined the Motorola European Center for Research and Development, Geneva, Switzerland, where she designed integrated circuits applied to telecommunications. In 1990, she joined EPFL as a Senior Assistant at the "Chaire des Circuits et Systèmes" (CIRC) where she was involved in impedance broadband matching. Since 1995, she has been responsible at the RFICs Group, EPFL, for RF activities. She has been the technical project manager of the European projects, CTI projects, and the Swiss National Science Foundation projects dedicated to RF wireless micropower sensor networks and mobile phones. Since 1998, she has been a Lecturer at EPFL in the area of RF circuits, electric filters, and CAD tools. Since 2006, she has been a "Maître d'Enseignement et de Recherche" (MER), EPFL. She is an author or coauthor of four scientific books and 50 scientific publications. Her current research interests include low-power analog circuits, biomedical remotely powered sensors, and electric filters.

Yusuf Leblebici received his B.Sc. and M.Sc. degrees in Electrical Engineering from Istanbul Technical University, in 1984 and in 1986, respectively, and his Ph.D. degree in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000–2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, Dr. Leblebici has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of 4 textbooks, namely, Hot-Carrier Reliability of MOS VLSI Circuits (Kluwer Academic Publishers, 1993), CMOS Digital Integrated Circuits: Analysis and Design (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications (Springer, 2007) and Fundamentals of High Frequency CMOS Analog Integrated Circuits (Cambridge University Press, 2009), as well as more than 200 articles published in various journals and conferences. He has served as an Associate Editor of IEEE Transactions on Circuits and Systems (II), and IEEE Transactions on Very Large Scale Integrated (VLSI) Systems. He has also served as the general co-chair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He is a Fellow of IEEE and has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.