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A New Built-In Defect-Based Testing Technique to Achieve Zero Defects in the Automotive Environment

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Abstract Efficient screening procedures for the control of the defectivity are vital to limit early failures especially in critical automotive applications. Traditional strategies based on burn-in and in-line tests are able to provide the required level of reliability but they are expensive and time consuming. This paper presents a novel built-in reliability testing methodology to screen out gate oxide and crystal related defects in Lateral Diffused MOS transistors. The proposed technique is based on an embedded circuitry that includes control logic, high voltage generation, and leakage current monitoring. The concept, advantages and the circuit for the proposed test procedure are described in very detail and illustrated by circuit simulation.

Keywords Gate stress test · Gate oxide reliability · Crystal defects · Burn-in · Low side switch

1 Introduction

The ability to control the random defectivity of a product during its life cycle becomes more and more vital especially in the automotive field, where the drive towards "zero-defects" is very stringent. In fact, due to the large number and critical functions of integrated devices in a car, random failures occurring in the field may have immediate disastrous consequences for the device manufacturer, which could be faced among other with safety issues for the car passengers, as well as expensive call back actions of the unreliable parts [2, 10, 12].

In recent years, due to the implementation of efficient design for reliability strategies, wear-out failures almost disappeared in integrated devices during the typical life cycle of a car ranging from 10 to 15 kilo-hours. Stated otherwise, the majority of the reliability issues that are observed at present in properly designed products, integrated into well matching and well controlled processes, mainly occur due to processing incidents and process-related defects, e.g. in the form of particles, lithography, or defects [11].

In particular, gate oxide defects and crystal defects are a major constraint in the development of reliable automotive devices because of the extensive use of large gate and junctions areas for the power devices. As a typical example, Fig. 1 shows the case of a multiple low side power switch for motor management, where 65% of the chip area is occupied by Lateral Diffused MOS transistors (LDMOS), while the remaining 35% by the Low Voltage (LV) circuitry. It is well-known that some process steps are more susceptible to increase the defectivity. The statistical analysis reported in Fig. 2 shows that the occurrence probability of gate oxide and crystal related defects is relevant if compared to the total amount of defects that can be introduced during wafer processing. Epitaxial deposition, polysilicon deposition in shallow trench isolations together with shallow trench etching are critical steps for the crystal and gate oxide quality. Furthermore the reliability of the gate oxide is affected by polysilicon deposition.

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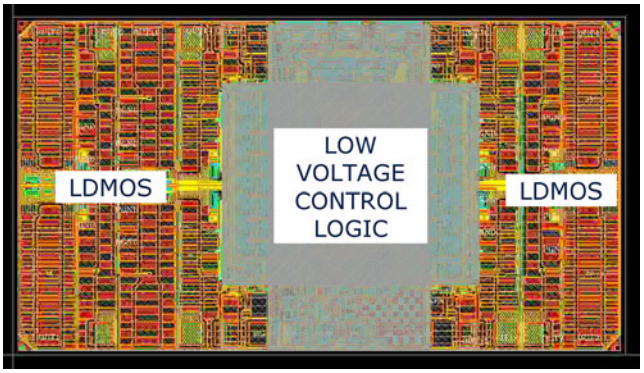

Fig. 1 LDMOS area occupation for a typical automotive application

Gate Oxide and Crystal Defects. According to the usual defective oxide classification, Class A includes such oxides, which are expected to fail (usually due to pinholes) for an applied field strength EBD (Electric field Break-Down) lower than 1 MV/cm. Class B includes the so-called extrinsic oxides that fail for an EBD lower than the intrinsic value, and Class C includes those oxides, which fail at an EBD above 10 MV/cm (for the thickness range of interest in this paper) due to intrinsic dielectric breakdown. At present the required failure rate during the life cycle of the product is assured by properly designed screening procedures before and after packaging of the chip, which force oxides in the Class A and B to fail, without introducing any substantial pre-damaging of the robust subpopulation [1].

Crystal defects (e.g. dislocations and stacking faults) can be either inherently present in the bulk silicon, or generated during some critical process steps like epitaxial growth, implantation, and the formation of shallow trench isolations. During the lifetime of a device, crystal defects can coalesce or act as a gettering site for dopant atoms and contaminations. This can result into the formation of local highly conductive paths, which under some circumstances can heavily affect the performance of the integrated circuit. This is in particular the case of LDMOS, where the presence of crystal defects in the active area can cause an

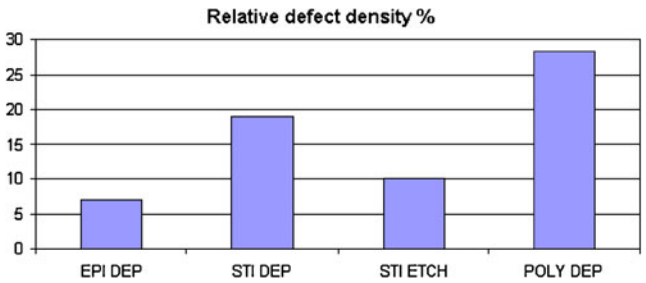

Fig. 2 Relative defect density introduced at critical process steps (EPI DEP = epitaxial deposition, STI DEP = polysilicon deposition in shallow trench isolations, STI ETCH = shallow trench etching, POLY DEP = polysilicon deposition)

increase in the source to drain leakage currents, or a significant reduction of the source to drain breakdown voltage [6, 9].

Screening Methodologies. Nowadays, the most common procedure to screen gate oxide defects at chip level is still the so-called gate stress test (GST), where a high voltage pulse is applied through an Automatic Test Equipment (ATE) to dedicated test pads of the LDMOS gate [5]. Subsequently, the eventual occurrence of the oxide breakdown is detected by the measurement of the leakage current through the gate oxide. The effectiveness of this methodology is due to the fact that GST provides high acceleration factor. However, after packaging, the accessibility of dedicated test pads becomes very limited, such that additional gate oxide screening is usually carried out in the form of a burn-in of the packaged devices at nominal supply voltage, at a junction temperature ranging from 125 to 140°C, and for a duration ranging from 24 to 48 h. In this case, an eventual gate oxide breakdown is detected indirectly either by a parametric, or by a functional test of the device.

The correlation between the presence of crystal defects and the increase of the transistor leakage current by various orders of magnitude is reported in literature [6, 9]. For this reason, screening for crystal defects is usually accomplished by measuring the drain leakage current when the device is biased under subthreshold conditions after applying a high voltage pulse to the drain terminal. This procedure is usually defined as Drain Leakage Test (DLT).

An excessive drain leakage current is considered to be a signature of a defect and the device is scraped if its value is higher than a given threshold. Unlike gate oxide defects, the crystal defects to be screened out may be very different in nature and affect different regions of the LDMOS. This implies that the voltage pulse applied during the DLT to enhance the leakage current due crystal defects may produce just negligible or none effect. Therefore, for practical applications, DLT cannot completely be used instead of the traditional burn-in under biased drain. Furthermore, the DLT can only be used for LDMOS, whose drain nodes can be accessed through external pins, such that inaccessible LDMOS remain untested.

Limitations of the Traditional Screening Methodologies. The main limitations of these traditional approaches are well-known. On one side they need expensive ATE, they require dedicated contact pads and overhead circuitry inside and outside the chip, they have very limited parallelization capabilities and finally they could be impossible after device packaging. On the other side, burn-in requires expensive equipment (load boards, control electronic, and thermal chambers), needs long testing times due to the limited acceleration factor, has limited accessibility to the

points of interest, has to be carried out on finished devices and finally it still requires expensive parametric and functional tests that often exhibit a limited testing coverage. In addition, the numerous manipulations of the devices increase the risk of pre-damaging due to electrostatic discharges.

The New Built-In Defect-Based Technique. In order to solve these limitations, a new approach to the screening of defective gate oxides and junctions of LDMOS is presented, which is based on dedicated embedded circuitry to perform on chip the voltage stress and the measurement of the leakage current through the stressed device. Due to the fact that it relies on built-in circuit, the proposed solution can be applied both at chip level and to packaged devices, targeting directly the point of interest. Furthermore, since the whole process is managed by an internal digital circuitry, it does not require any additional testing equipment and can be run in parallel on a very large number of devices.

In this paper, the traditional GST approach in use nowadays for several automotive products is presented in Section 2.1, to point out requirements and limitations. In Section 2.2, the concept behind the novel built-in GST is defined together with its main constituting blocks. Section 2.3 describes in very detail the circuit solution used for the built-in GST unit with special focus on design solutions adopted to make the coexistence of different type of devices on the same design possible. In Section 2.4, the physical principles and models are presented, by which the duration and the voltage levels of the high voltage pulse used in the built-in GST have been calculated to attain the required acceleration factor. Section 3.1 describes the challenges posed by the traditional DLT, and in section 3.2 and 3.3 it is described the solution proposed together with its circuit implementation respectively. In Section 4, the accuracy of the leakage current measurement unit is discussed in conjunction with the illustration of the circuit overhead (area, complexity) required by the novel built-in test methodology. Finally, Section 5 shows the results of the validation of the proposed design by transient SPICE simulations.

2 Built-In Test for Gate Oxide Screening

2.1 Traditional Gate Stress Test Method

Traditionally, GST is performed accessing the gates of power FET-switches by contacting needles of an ATE probe-card on one or more test pads. A typical configuration of such a circuitry is shown in Fig. 3.

Several HV-LDMOS transistors might share the same gate stress test pad by using decoupling diodes (D4 and D5 in Fig. 3). The zener diode Z is required to protect the gate driver low voltage N-MOS and P-MOS transistors from high voltages. The series resistor R is needed between the gate driver and the gate stress test pad in order to limit the current during the high voltage gate stress. The gate driver circuit design prevents current flow into the driver during the gate leakage test by the use of the optional diode D3. Passive gate-discharge circuits are disabled by additional test pads during gate leakage test (e.g. test pad TP1 in Fig. 3).

The gate is stressed by a high voltage pulse applied through the ATE. The difference between the current flowing into the GST pad before and after the stress is calculated. If the difference exceeds a specified threshold, the device is scrapped.

Issues Related to the Traditional GST Methodology. The popularity of this solution is justified by the fact that is very simple to be implemented, but on the other hand it does not solve a multitude of challenges at different levels.

Design level—The diode D3 in Fig. 3 limits the driving voltage of the gate of the LS-SWITCH. Therefore, in order to get the same Ron performances, the area of the HV-LDMOS has to be increased. Moreover, the resistance R is critical for applications where fast turn-on/off switching time of the transistor is required.

Wafer level test—The wafer-probecard requires extra needles exclusively dedicated to the GST. In addition, one has to rely on external Automatic Test Equipment (ATE) in order to perform a non trivial measurement. This fact impacts the test cost and reduces the capability to screen several devices at the same time (parallelization).

Package Level test—Since the stress introduced by bonding and plastic molding compounds can affect the gate oxide reliability, performing GST is essential after packaging, as well. However, for pin number reduction and in order to avoid electrostatic discharge events, both the GST and the TP1 pad are not bonded so that the gates of the HV-LDMOS switches are no longer accessible.

Burn-in level test—Static temperature stress under constant bias voltage is a way to accelerate the Time Dependent Dielectric Breakdown (TDDB) during burn-in. An issue related to this approach is that the stress is applied at the same time even to non-defective gate oxides. This reduces the residual lifetime of the surviving gate oxides. Moreover, the detection of possible breakdown events can only be performed indirectly through a parametric or functional test, since accurate current leakage measurement is no longer possible.

2.2 The Novel Built-In GST Concept

Description. The proposed solution, called Built-in GST (BI-GST), consists of the integration of all the functionality required to perform a GST into each device. Following this

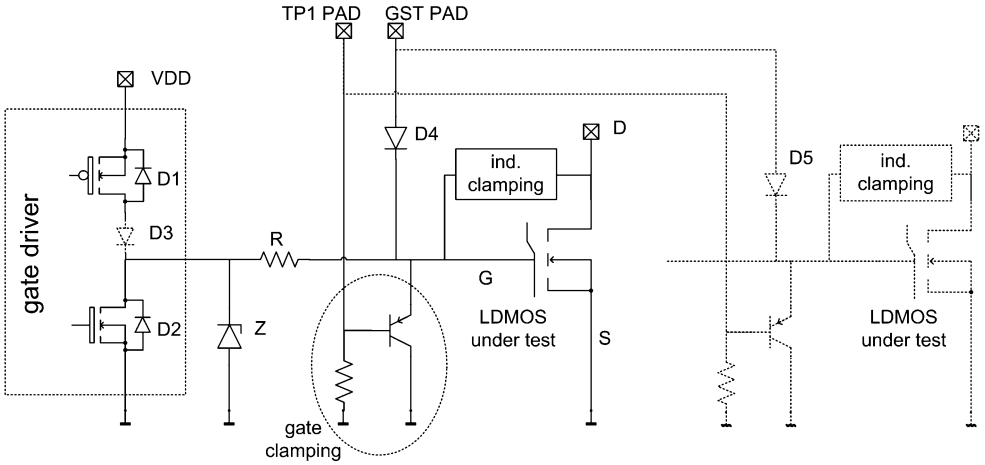

Fig. 3 Traditional gate stress test scheme (GST)

approach, every chip should become responsible for its own stress test. The principles of the implementation of this solution are presented in Fig. 4.

In order to save additional pads/pins for stressing, the high voltage, which has to be applied to the gate oxide of the LDMOS, is forced via the battery pin V_S. The stress sequence is enabled by a command sent via a serial interface. A digital controller asserts the GS_ISO and GS signals controlling respectively the protection switch and the stress switch according to the basic waveforms show in Fig. 4. The former is responsible for the disconnection of the gate driver unit from the LDMOS gate. The latter controls the application of the stress voltage on the gate. The protection switch, the gate clamping and the inductive clamping are designed in such a way that no current flows through them during the gate stress. The current I_{leak}, flowing from the battery pin to the gate, is measured, mirrored by the current mirror and compared with a threshold current I_{th} by the current comparator. The current I_{th} is generated internally by a digitally programmable current source, and it is set to a value proper to discriminate the intrinsic gate leakage current from the leakage current resulting from a breakdown. The threshold current is typically set to 1 μA based on results obtained from dedicated breakdown experiments carried out on test structures.

The result of the comparison is a digital signal, COMP_O that is sent to the external world via a serial interface, indicating whether the leakage current through the gate oxide is higher than a given threshold current.

Advantages of the Proposed Solution. The BI-GST approach is beneficial under many aspects. Firstly, it reduces the dependency on external ATE, reducing at the same time the testing time and the resulting testing cost. This is due in particular to the fact that the average testing time required

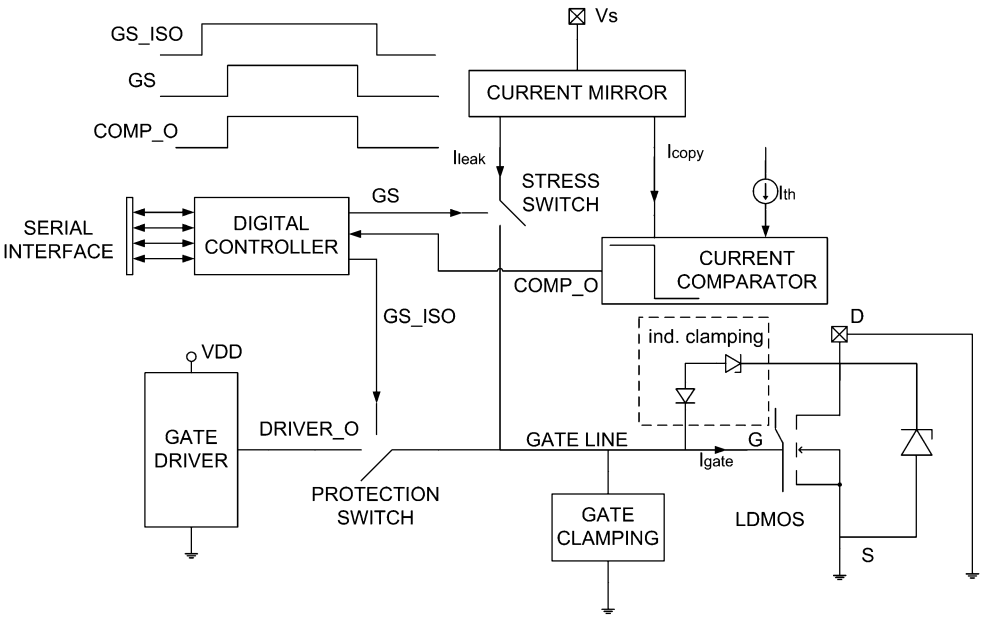

Fig. 4 Working principle of the solution implementing BI-GST

by the BI-GST approach is shorter than in the traditional one, and that the BI-GST approach introduces the capability to test more devices in parallel. Furthermore, the BI-GST approach enables the manufacturer to perform a targeted GST after packaging of the device and even during high temperature storage (e.g. burn-in), what it has not been possible until nowadays by the use of the traditional GST solution. Of course, the BI-GST represents a valid solution if the increased efforts for the additional silicon area are compensated by the benefits in terms of decreased test costs and improved reliability of the devices in the field.

2.3 Circuit Description

Several design challenges arise for the implementation of the BI-GST concept of Section 2.2. In particular, the design has to handle high voltages, perform accurate current measurements without introducing significant voltage drop and use a silicon area which is much smaller than the typical size of the LDMOS to be screened.

Unfortunately, all these requirements cannot be simply fulfilled at the same time by a standard HV or CMOS technology. In the most recent BCD technologies high voltage (HV-DMOS), medium voltage (MV-CMOS) and low voltage (LV-CMOS) transistors are available and can be combined on the same die.

Figure 5 shows the detailed schematics of the circuitry, where the voltages have been annotated for the critical nets both during normal and built-in GST operation.

In normal operation the protection switch is closed and the stress switch is open. The PROTECTION SWITCH is based on a transmission gate engineered by HV-LDMOS (P2-N3 in Fig. 5). This configuration is required such that the switch can operate in normal conditions in the voltage range from 0 V to VDD. The stress section is completely transparent, such that no constraints have to be imposed to the design of the gate driver.

During the BI-GST stress, the protection switch is off and the stress switch is on. The pull-down transistor N2 of the gate driver is constantly on, forcing the net DRIVER_O to ground. The node P, grounded by N4 during normal operation, becomes floating when the GS_ISO signal is asserted. To keep the protection switch off, N3 should have the gate to ground, while the gate of P2 needs to follow the gate line voltage.

The STRESS SWITCH is implemented by P6 and P5. The switch is enabled by generating a voltage drop, V_S-V_{BIAS}, at the node BIAS. Being P4 matched to P6, and P8 to P9, both P5 and P6 try to source current to the gate line and to the node P. Since both are in the high impedance state, the voltage at these nodes will rise, saturating P5 and P6 to a value equal to V_S-V_{GSP9}. Z1 protects P2 against possible transient overvoltages which could damage the gate oxide. This bias technique limits the charging current trough P6 and P5 avoiding fast transients, dangerous for parasitic current injection and protecting P9 from high current flow. The pull-up resistor R4 is responsible for discharging the BIAS node after the completion of the stress phase.

The performance of the CURRENT MIRROR affects the accuracy of the overall current measurement. Two different errors are introduced: a voltage error V_e, defined as the difference between the applied voltage at the battery pin V_S

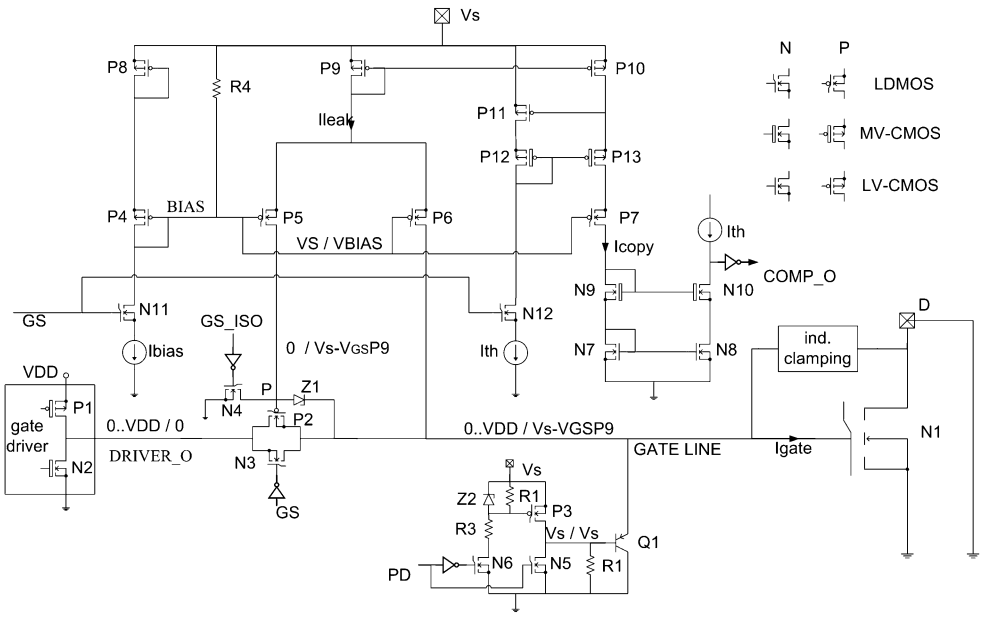

Fig. 5 Circuit description of the solution implementing BI-GST

and the voltage really applied on the gate line V_{GATE}, $V_e=V_S-V_{GATE}\cong V_{GSP9}$, and a current error I_e, defined as the mismatch between the current flowing into the gate I_{leak} and the current I_{copy} that enters the comparator, $I_e=I_{leak}-I_{copy}$. Both error sources have to be kept below the limits imposed by the accuracy requirements for this application. In order to reduce the inaccuracy of both sources, LV-PMOS devices P9-P10 have been introduced. This kind of device in fact, offers the best matching performance and smallest threshold among all others. The drawbacks are their relatively low output impedance and their poor voltage capabilities. To overcome these limits a cascode current mirror with low input voltage requirement has been chosen [3, 4, 7, 8]. The configuration used in this paper is called regulated cascoded circuit with reference tracking [4]. The original design has been modified here in such a way that the reference current does not replicate the measured current I_{leak}, but the current I_{th} that is used for the current comparator.

This modification is necessary because in general I_{leak} is too small to operate properly the current mirror. P10 copies the leakage current I_{leak} with unity gain by avoiding any channel length modulation effect when I_{leak} is of the same order of magnitude as I_{th}. In fact in this situation the feedback loop forces the drain voltages of P10 to match the drain voltage of P9. This solution increases the accuracy of the current mirror close to the range of interest (i.e. around I_{th}) for the current comparator.

Recycling of LV-MOS devices connected directly to the battery supply pin Vs is made possible by the fact that the common LV-CMOS p-well for such devices can be connected to floating potentials. In particular, the p-well of all LV-PMOS devices has been connected to the BIAS node.

The gate discharging device Q1 is disabled by the application of V_S voltage on its base. P3 is switched on by the voltage drop generate across the zener Z2.

After the application of the stress, GS is disabled and the gate line is discharged by closing N3 and connecting N2.

The additional circuit required for the implementation of the BI-GST doesn't affect the performances of the original circuit in terms of switching speed and power consumption because of the small additional RC load introduced. In fact the protection switch has been designed to operate with an ON-resistance of few hundred Ohms and the capacitive load added on the gate line is negligible if compared with the gate capacitance of the LDMOS under test.

2.4 Calculation of the Stress Pulse Duration

For the calculation, it is assumed that a burn-in carried out at a temperature T_{stress}, at nominal supply voltage V_{op} and with duration D_{BI}, delivers the required failure rate in the field. Thus the problem to be solved for the built-in GST is the calculation of the high voltage pulse duration t_{pulse} (at a voltage V_{pulse}), which delivers an equivalent stress as in the burn-in defined above. The conversion can be made, once the acceleration factors related to the failure mechanism and to the stress factors (in this case the electric field in the oxide E_{ox} and the oxide temperature T) are known.

The dielectric breakdown due to extrinsic defects is usually attributed to defects at or near the Si/SiO_2 interface. This is the case for instance of decorated stacking faults or local discontinuities in the oxide caused by metallic precipitates [1]. Therefore the defect-induced breakdown is modeled accurately by the effective thinning concept, where defects are represented as a localized thinning of the oxide described by the effective oxide thickness X_{eff} at the weakest spot in the oxide. This concept also covers frequent local defects related to asperities at the interface and localized areas with anomalous chemical composition (e.g. particles).

According to the general reliability design rule in presence of a local thinning, it is assumed that under operating conditions, the density of the Fowler-Nordheim current has to be negligible. Therefore the electric field strength across the thinning has not to exceed 7 MV/cm. In other words, the screening procedure has to be designed to eliminate all those devices, where E_{ox} exceeds 7 MV/cm under usual operating conditions, without introducing any substantial pre-damaging of the robust subpopulation.

At microscopic level, the physics behind time dependent dielectric breakdown of extrinsic oxides is rather complex and leads to a strong statistical spread of the lifetime depending on the nature and on the density of oxide defects (which are either native or created during the stress) [1]. Nevertheless, there is a general consense on the fact, that in the case of oxides thicker than four nanometers, the lifetime due to dielectric breakdown exhibits a temperature acceleration factor AF_T that is described by the Arrhenius-like relation

$$AF_T = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_{op}} - \frac{1}{T_{stress}}\right)\right) \quad (1)$$

where E_A is the activation energy in the 0.4–0.6 eV range, k the Boltzmann constant, T_{op} and T_{stress}, the oxide temperature under operating and accelerated conditions, respectively.

Similarly, the field acceleration factor AF_V is given by

$$AF_V = \exp\left(\gamma\left(E_{stress} - E_{op}\right)\right) \quad (2)$$

where γ is the field acceleration parameter (in the 1.5–2 cm/MV range), E_{op} and E_{stress} are the electric fields in the

field oxide under operating and accelerated conditions, respectively.

Combining (1) with (2)

$$t_{pulse} = D_{BI} \exp\left(\frac{E_A}{k}\left(\frac{1}{T_{op}} - \frac{1}{T_{stress}}\right) - \frac{\gamma}{X_{eff}}\left(V_{pulse} - V_{op}\right)\right) \quad (3)$$

yields the required pulse duration t_{pulse}.

For typical values of E_A, T_{op}, T_{stress}, γ, X_{eff}, V_{op} and for V_{pulse} in the range from 17 V down to 14 V, Eq. 3 delivers a pulse duration t_{pulse} in the range from 50 μs to 4 ms per hour burn-in. Thus, as an example, the pulse duration at V_{pulse}=16 V, equivalent to 48 h burn-in at 140°C, is 3 ms.

3 Built-In Test for Crystal Defect Screening

3.1 Traditional Drain Leakage Test Method

Traditionally, DLT is performed via direct access of the ATE to the drain of power FET-switches through pins. The configuration used for this test is shown in Fig. 6. Z_{ESD} is the zener diode used as an ESD protection for the output pad D. The DLT consists of three steps. Firstly, the LDMOS in turned off by forcing the gate to ground through the driver or the gate clamping. Then a high voltage pulse is applied to the pad D. Finally, the leakage current flowing into the D pin is measured by the ATE. The level of the voltage pulse has to be high enough to force the junctions affected by crystal defects into reverse breakdown, so that the local defect will possibly degrade and result into an increased leakage current. The voltage to be applied to D during the characterization of the leakage current, has to be sufficient to provide enough accuracy, but at the same time it should not exceed the threshold for the activation of unwanted parasitic conduction paths, which can be essentially of three types. In the first case, the leakage is produced by the inductive clamping. This current path can be blocked by switches or structures which increase the clamping voltage only during test mode (TM). The second cause is related to the zener diode Z_{ESD}, which can be forced into reverse conduction. Last, the leakage current can arise due to the intrinsic breakdown of the LDMOS. Therefore, the voltage applied during the characterization phase is usually 2 up to 5 V lower than the reverse breakdown voltage of the zener diode Z_{ESD}.

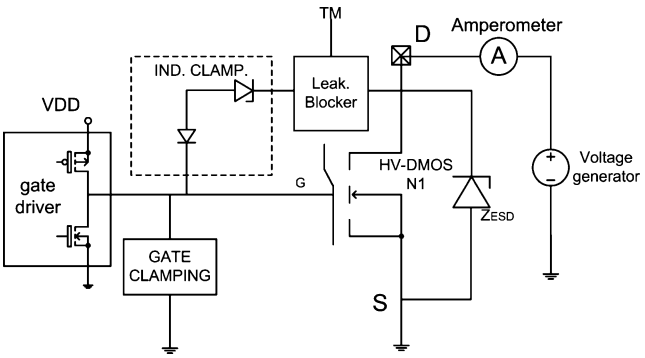

Fig. 6 Traditional drain leakage test scheme (DLT)

Issues Related to the Traditional DLT Approach. The main issue of the traditional DLT is related to the fact that the efficiency of the stress acceleration while applying a voltage pulse is questionable. Actually, even if the high voltage pulse forces weak junctions into the reverse breakdown, it might also not produce permanent local damages resulting into in an increased leakage current during the characterization phase. In fact, leakage currents through the crystal defects may be more efficiently increased by a continuous voltage stress at increased temperature, as it is the case during the burn-in. Under these circumstances, multiple accelerating effects can be activated, as local thermal damaging of the lattice, propagation of the crystal defect, or enhanced precipitation along the defect itself. However, the strongest limitation of this traditional approach is the fact that it requires that the drain contacts of the chip being biased over the whole duration of the burn-in, increasing in such a way the cost involved with the screening. In addition, this procedure can only be carried out, if the direct access to the drain contact is directly (and separately) ensured. Actually, the direct contact to the drain contact of LDMOS is just granted through the pins if they are used to drive external loads. Nevertheless, in the case of modern designs using large power transistors for internal purposes, this represent a major limitation, since the design of an addition pin just for testing purposed is rarely viable.

3.2 Integration of the Drain Leakage Test Functionality to the Built-In GST Concept

The solution proposed to implement the built in Drain Leakage Test (BI-DLT) makes use of the capabilities offered by the circuit for the BI-GST, introduced above. The realization of this additional test mode has been made possible by minor design changes, which have almost no impact on the required area overhead.

The design concept bases on the same principles as for the BI-GST, i.e. the use of an external high voltage source (provided through the battery pin), the implementation of a high impedance node and the measurement of the leakage current through the high impedance node. The solution is

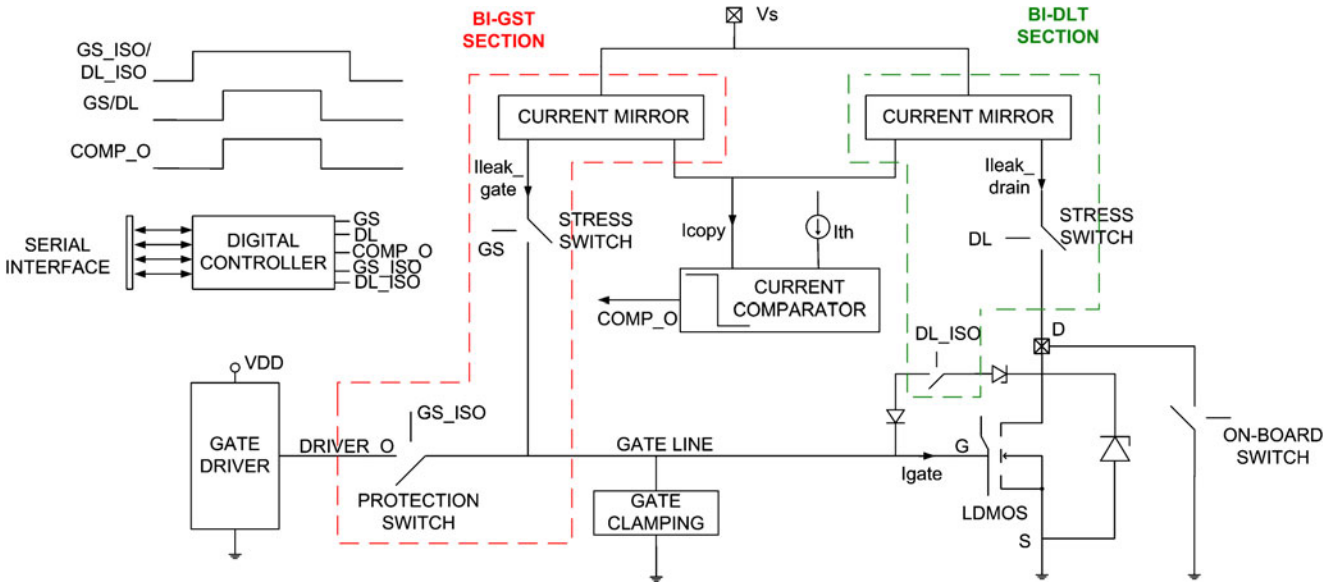

Fig. 7 Working principle of the solution implementing BI-GST and BI-DLT

illustrated in Fig. 7. After receiving the command to perform the test from a serial interface, a digital controller provides the necessary controlling signals. The signals DL and DL_ISO have been added to control the application of the test voltage on the drain and the opening of the inductive clamping. An on-board switch will connect the drain to ground during BI-GST and will leave it floating during BI-DLT. The current flowing into the drain I_{drain} is mirrored and compared with a threshold current I_{th} by the current comparator. I_{copy} is a replica of the gate leakage current during BI-GST and a copy of the drain leakage current during BI-DLT. The COMP_O signal will be forwarded via serial interface to the external world, indicating a leakage current higher or lower than the threshold current.

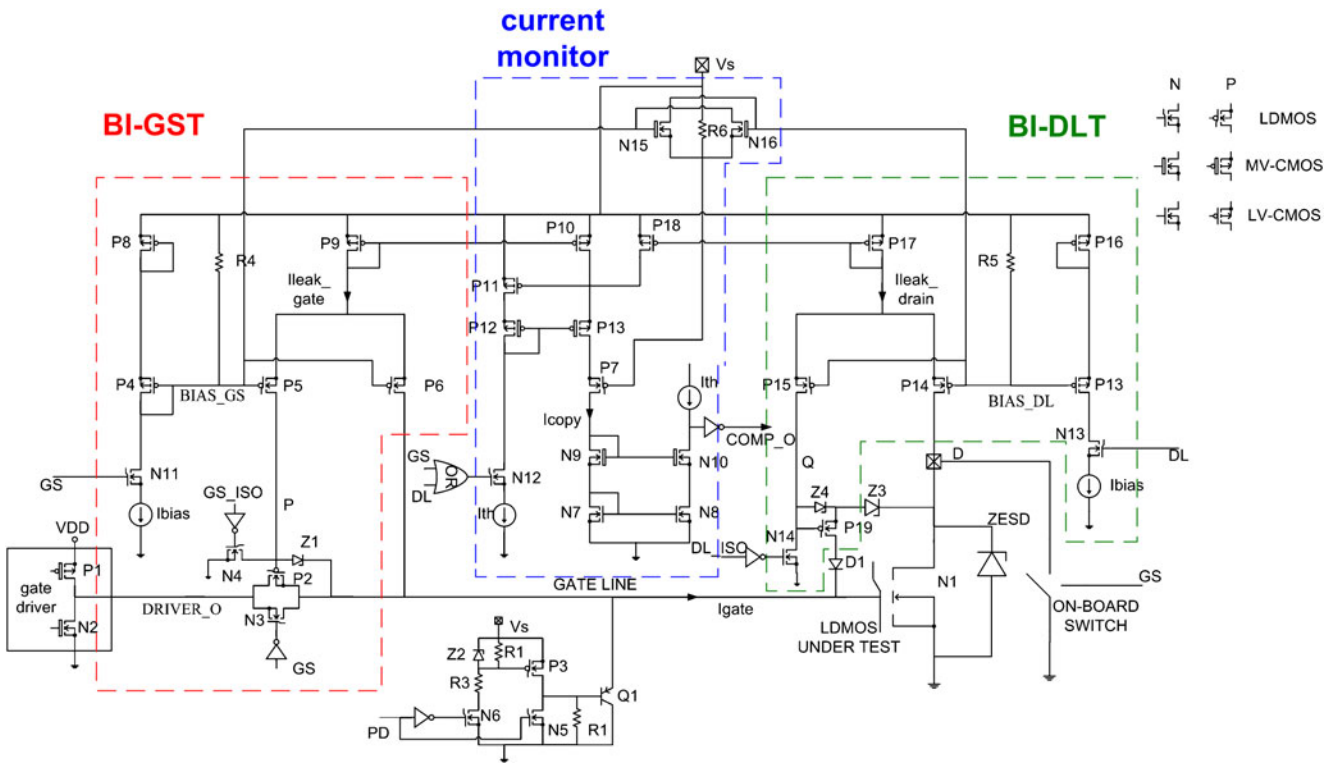

Fig. 8 Circuit description of the solution implementing BI-GST and BI-DLT

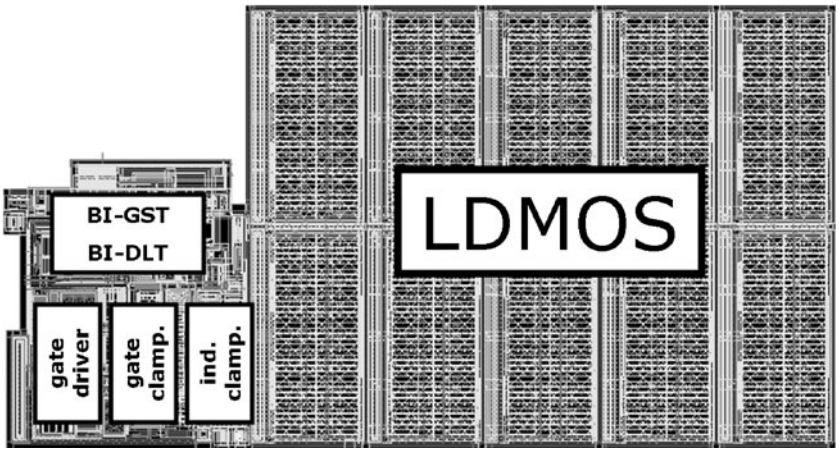

Fig. 9 Layout of the solution implementing BI-GST and BI-DLT

Advantages of the BI-DLT. The BI-DLT presents major advantages either in the case of it is used as standalone screening technique, or in conjunction with a traditional burn-in procedure.

The design solution proposed here for the standalone version refers to a LS-switch with direct access to the drain and source through external pins. Obviously, this design could be easily extended to the case of embedded LDMOS transistors without any direct access from outside. This just requires an additional connection to ground of the source terminal, as well as an isolation of the drain node to block any unwanted parasitic leakage current during the test.

As it was the case of the DLT, even the BI-DLT cannot completely replace the traditional burn-in screening procedure, due to the erratic behavior of the high voltage pulses used in both techniques to accelerate the degradation of possible leakages due to crystal defects. Nevertheless, since the BI-DLT has been integrated in a process for temperatures up to 200°C, it can be used very proficiently in conjunction with traditional burn-in storage under bias. In this case, BI-DLT just requires the high voltage to be supplied through the battery or any kind of high voltage capable pin. Operating the device in the BI-DLT mode would enable to monitor the time dependency of the drain leakage current at high temperature during the burn-in screening. The main advantages involved with this approach are a better insight into the degradation process over the whole duration of the screening, a better screening efficiency due to the monitoring capabilities of the leakage current during the burn-in (and not just at the beginning and at the end), and a relevant cost/time reduction of the screening procedure because the characterization can be

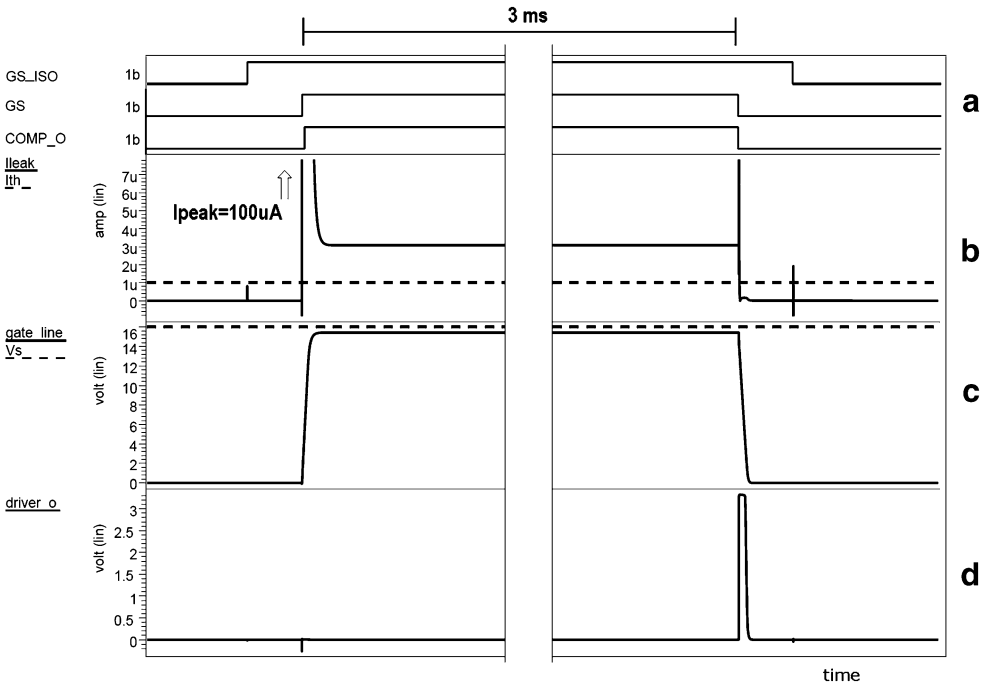

Fig. 10 SPICE simulation of (a) the timing of the control signals for BI-GST, (b) resulting current pulse at the gate during application of the high voltage pulse with a high-ohmic short circuit towards substrate of 5 MΩ, (c) high voltage pulse, and (d) net driver signal

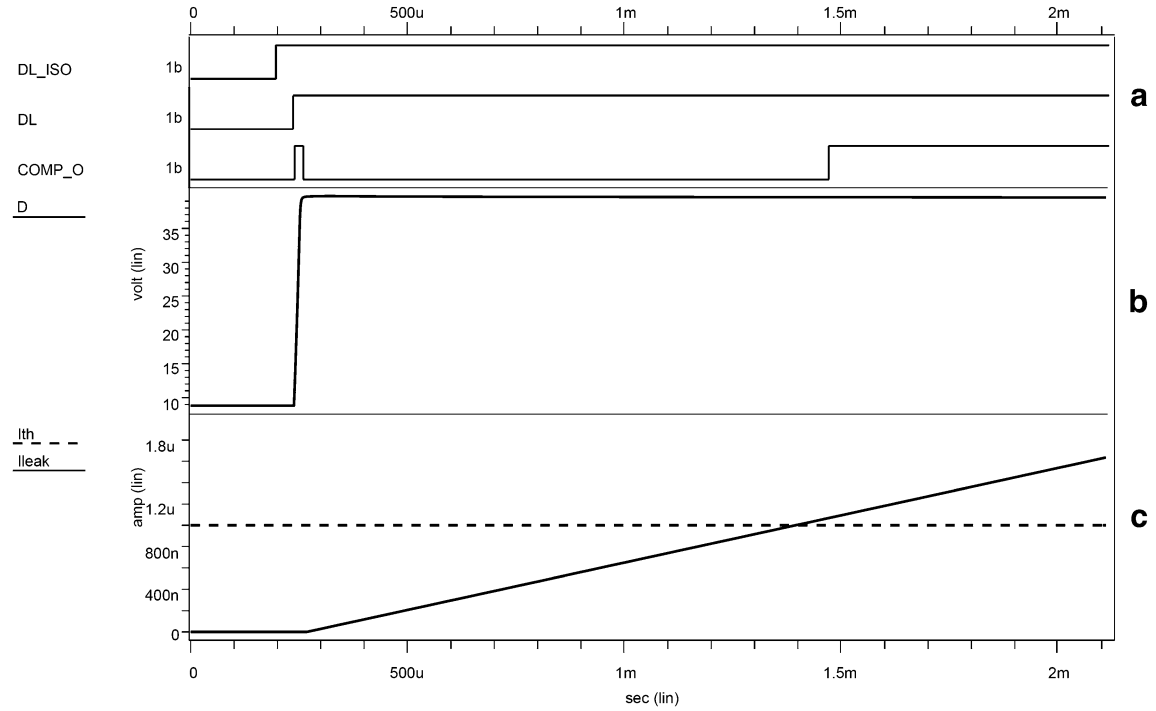

Fig. 11 SPICE simulation of (a) the timing of the control signals for BI-DLT, (b) voltage on the D node, (c) threshold current and applied current to simulate leakage

carried out on all devices at the same time (parallelization) and without the use expensive ATE equipment.

Finally, this also impacts very positively the development of optimized temperature profiles for crystal defects screening and the cost reduction of the burn-in test boards, which can be substantially simplified by the use of the digital serial interface already embedded into the circuit to be screened.

3.3 Circuit Description

The circuit added to perform the BI-DLT is an extension of the circuit used for BI-GST and its working principle is the same. Both sections work completely independently, in a sense that the operation of the BI-GST section is not affected by the BI-DTL, and vice versa. The only restriction is that both tests have to be carried out sequentially.

During BI-DLT, the gate of the LDMOS under test N1 is kept down by the driver or by the gate clamping circuit via Q1. Z3 and D1 are the inductive clamping circuit. In normal operation, when the inductive clamping is required to work, P19 is on, since its gate is kept to ground by N14. During the BI-DLT the gate of P19 is raised up to the test voltage that is also applied on the drain of N1. In this case the inductive clamping circuit is open and no leakage current can flow.

The current comparator circuit is used for both tests. For this reason it is activated selectively, depending on which test is needed.

Similarly, N15 and N16 provide an easy way to generate the lowest between the two voltages BIAS_GS and BIAS_DL. This voltage is used to turn-on P7 when one of the two tests is required.

4 Analysis of the Accuracy and of the Silicon Area Consumption

The accuracy of the leakage current measurement is defined by the local matching performances of current mirrors P9-P10, P17-P18 and N7-N8 in Fig. 8. Intra-die, chip-to-chip, wafer-to-wafer, and lot-to-lot variations play a minor role in the decision which relies on the behavior of equally designed devices within a chip. The variance of the relative current differences in a current mirror is given by:

$$\sigma^2_{\Delta I/<I>} = \frac{\sigma^2_{\Delta V_T}}{(V_{GS} - V_{TH})^2} = \frac{B}{I_D L^2} \tag{4}$$

where

$$\sigma_{\Delta V_T} = \frac{A}{\sqrt{WL}} \tag{5}$$

represents the threshold mismatch of the transistors, while A and B are technology-dependent constants. The fact that the variance is inversely proportional to the bias current and to the channel length squared represents a drawback for the

present application, where small currents are measured and a small voltage drop is used to minimize the voltage error V_e. All current mirrors have been designed in order to reach a current mismatch better than 4% at 1 μA bias current.

Furthermore, the contribution of the inaccuracy of the I_{th} has to be considered for the overall accuracy estimation. I_{th} might be generated internally, such that its accuracy is typically within 2–3%.

This solution has been introduced in a typical LS-SWITCH application, designed to obtain R_{ON}=0.4Ω. The additional area occupied by the built-in test circuitry is 10% of the area occupied by a single LS-SWITCH as shown in Fig. 9. Further, the reduction in terms of reliability due to the additional circuit is negligible, since the gate oxide area associated with built-in test unit is a factor of 500 smaller than the gate oxide area in a HV-LDMOS. The relative area overhead is reduced if more than one LS-SWITCH could be tested in parallel.

The small size of the stress circuitry and the fact that no device is stressed during stress, except for the LS-SWITCH, makes the solution attractive with negligible risk for additional reliability problems.

5 Spice Simulations

Figure 10a shows the timing of the most significant control signals introduced in Section 2.2 during the high voltage stress phase for the BI-GST. Fig. 10b represents the current injected to the gate when applying the high voltage pulse.

The effect of a leakage current I_{leak} through the gate oxide has been reproduced by means of a 5 MΩ resistor R_{leak} between the gate node and ground. In this example, the current I_{th} has been set to 1 μA. Figure 10c shows the resulting waveform of the high voltage pulse with V_{pulse}=16 V and a duration of 3 ms. The rise and fall time of the pulse are controlled by the current required to charge the gate line to V_S-V_{GSP9} (set here to 100 μA). Once the gate has been charged, the remaining leakage current I_{leak} flows only into R_{leak}. Since I_{leak}>I_{th}, the COMP_O is set during BI-GST indicating that the leakage is too high. Finally, Fig. 10d shows the voltage of the signal DRIVER_O at the output of the gate driver. It is 0 V during the application of the stress and rises to V_{DD}-V_{GSN3} when the gate line is discharged through N2.

Figure 11 shows the simulation results for a typical BI-DLT cycle. The digital control signal and the output of the comparator are represented in Fig. 11a. The voltage on the drain of the LDMOS rises till the test voltage, 40 V in this case, as soon as the DL signal is asserted (Fig. 11b). The leakage from the drain has been simulated with a current source that generates the current ramp I_{leak}. Immediately after the value of the leakage crosses the value of the threshold current (Fig. 11c), the COMP_O flags an excessive leakage. The initial activation of the COMP_O signal that immediately occurs after the DL signal becomes active is due to the current flow necessary to charge the parasitic capacitance on the D node.

6 Conclusion

A novel built-in approach has been proposed to screen out defective gate oxides (BI-GST) and crystals defects (BI-DLT) in Lateral Diffused MOS transistors in integrated circuits for automotive applications. This technique is based on a programmable embedded circuitry for built-in testing, which provides high voltage pulse-stressing and accurate quantitative measurement of the leakage current through the gate oxide or through the drain. The test sequence is controlled by internal logic and the unit communicates to the outside world through a serial interface. The peculiarities of the circuit design have been discussed with particular focus on the design solutions adopted for high-voltage operation and accurate current measurement by dedicated current mirrors.

Both BI-GST and BI-DLT have been shown to be a valid alternative to the traditional approaches relying on automatic test equipment (ATE) for screening and burn-in. In opposite to the traditional techniques, these new techniques can be applied both at chip level as well as in packaged devices, and do not require sophisticated ATE to be used. This, in conjunction with the fact that they can be performed in parallel in several devices, results at the same time in a more targeted stress than for the traditional burn-in and in a noticeable decrease of the costs involved with the screening. BI-GST and BI-DLT just imply a moderate silicon surface overhead in the 10% range of the area of a single LDMOS, which has a negligible impact on the reliability of the whole circuit.

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